REMARKS

Applicant thanks the Examiner for acknowledging the claim to foreign priority and for confirming that the certified copy of the priority document was received by the U.S.P.T.O.

Applicant notes that the Examiner has not provided a signed copy of Form PTO-1449 for the Information Disclosure Statement filed on November 21, 2001. Applicant requests the Examiner to acknowledge consideration of all documents submitted with this IDS.

Claims 1-4 and 6-8 are all the claims pending in the application.

Drawings

To overcome the Examiner's objections to the drawings, Applicant submits the attached proposed drawing corrections for Figures 1, 6 and 9 and new Figure 12. Figures 1, 6 and 9 now label the analog switches disclosed at pages 10, 21 and 22. Pages 10, 21 and 22 have been amended to provide reference numerals to the specification disclosed analog switches corresponding to those illustrated in Figures 1 and 9.

New Figure 12 illustrates the analog switches composed of p-channel transistors and n-channel transistors provided in the gray shade voltage selecting circuits 31, 32, as explained at page 23 of the subject application.

Claim Rejections - 35 U.S.C. § 112

Claim 1 stands rejected under 35 U.S.C. § 112, first paragraph. There is no basis for this rejection since the claims as originally filed are part of the specification (see MPEP § 608.01(l))

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and clearly convey to one skilled in the relevant art that the inventor had possession of the claimed invention at the time the application was filed. Since claim 1 fully supports the inventor's possession of the claimed invention at the time of filing, the Examiner must withdraw this rejection. For the Examiner's convenience, Applicant refers the Examiner to the discussion of Figure 5, beginning on page 14, line 15, and ending on page 15, line 20, and the discussion of Figure 6, beginning on page 16, line 26, and ending on page 18, line 21.

Claim 1 stands rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for allegedly omitting essential elements. This rejection is traversed. Applicant accurately claims the improvements to a driving circuit of a display device for displaying a plurality of gray shades based on inputted digital image data which includes the combination of a gray shade voltage generating means, a gray shade selecting means, an operational amplifier, and a voltage adjusting means. Claim 1 particularly points out and distinctly claims the subject matter which Applicant regards as his invention. The Examiner's attention is respectfully directed to the language of § 112 (second paragraph). This section requires that the claims particularly point out only that which "applicant regards as his invention". As in this case, where the invention is an improvement to a driving circuit, only the improvement need be claimed and that is what is claimed. It is unnecessarily limiting in view of the prior art to specify the particular elements of Figure 5 in claim 1. Claim 1 clearly does not omit any essential element of the novel claimed invention.

Additionally, elements of claim 1 and its dependent claims are in "means plus function" format. These elements recite the stated function of the claimed elements and pursuant to § 112

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(paragraph 6) will retain the "means plus function" attribute only if specific structure is not associated with the stated means within the claim itself. The statute explains that the structure of a recited "means" is the structure described in the specification for carrying out the stated function and its equivalents. There is no requirement, and in fact it is the antithesis of a "means plus function" element, for the claim to be expressly restricted to structure corresponding to claimed "means plus function" elements.

Applicant therefore requests that the Examiner withdraw this rejection.

The Examiner also rejects claim 1 under § 112, second paragraph, as being indefinite. in the language associated the claimed "operational amplifiers". Claim 1 has been amended to overcome this rejection.

Claim Rejections - 35 U.S.C. § 103

Claims 1-4 and 6-8 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art ("AAPA") in view of Yanagi, U.S. Patent No. 5,929,847. Applicant traverses this rejection.

Claim 1 is independent with claims 2-4 and 6-8 depending therefrom. Regarding claim 1, the Examiner admits that the AAPA does not disclose a voltage adjusting means. The Examiner argues, however, that "Yanagi teaches, referring to Fig. 17, the voltage generating circuit having the control signals Sac and Sdc (the digital image data), the operational amplifier (op-amp) OPa, a resistor R3 connected at node Vy and source of transistor SW1 a signal POL (low order bit), the output voltage Vy = Vdc +Vac (a voltage rise) (see col. 30, lines 55-67)."

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The above deficiency of the AAPA is not overcome by Yanagi. Figure 17 of Yanagi illustrates an example in which a common electrode drive circuit regulates control signals S_{ac} and S_{dc} with a voltage and is provided as an alternative to a gray-scale voltage generating circuit for a display device. (Yanagi, col. 29, line 64 - col. 30, line 2). The present invention, however, relates to a driving circuit of a display device for displaying a plurality of gray shades based on inputted digital image data.

Since the generating circuit of Fig. 17 in Yanagi does not relate to a gray-scale display device, this portion of Yanagi does not teach or remotely suggest adjusting a voltage output from an operational amplifier in response to the low order bits of a digital image data. The voltage generating circuit of Yanagi's Fig. 17 merely adds or subtracts an ac voltage to a dc voltage in response to the switching of switches SW_1 and SW_2. (Yanagi, col. 21, lines 1-5).

Referring to the gray-scale voltage generating circuit embodiments illustrated in Figures 8, 10, 12, and 13 and described in Examples 6-9 of Yanagi, Applicant notes that Yanagi still does not overcome the above deficiencies of the AAPA. For example, as shown in Figure 13, output voltages V_a and V_b are controlled by level control circuit T in response to control signal POL and not by a low significant bit of a digital image data, as required by claim 1.

Because neither the AAPA nor Yanagi, nor their combined teachings, discloses or suggests a voltage adjusting means as claimed, one of ordinary skill in the art would not (and could not) have found it obvious to combine these two references to produce the unobvious

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device of Applicant's claims. Thus, Applicant requests the Examiner to withdraw the rejection of parent claim 1 and dependent claims 2-4 and 6-8 under 35 U.S.C. § 103.

Since claim 1 is generic, upon allowance of claim 1, all non-elected species claim, 5 which depends from claim 1 should also be allowable. So too should non-elected species claims 9-13 wherein claim 9 is independent and claims 10-13 dependent thereon.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Applicant hereby petitions for any extension of time which may be required to maintain the pendency of this case, and any required fee, except for the Issue Fee, for such extension is to be charged to Deposit Account No. 19-4880.

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

The specification is changed as follows:

After the eight paragraph of page 8, please add the following new paragraph:

Fig. 12 is a schematic block diagram of an analog switch provided in gray shade voltage selecting circuit.

In the last paragraph of page 9 (which bridges over to page 10), please delete that paragraph and replace it with the following:

The driving circuit is further provided with a gray shade voltage generating circuit 6 used to divide gray shade voltages including 10 voltage values from V0 to V9 and to input 128 gray shade voltages having either of positive polarity or negative polarity. It is also provided with a first gray shade voltage selecting circuit 7 and a second gray shade voltage selecting circuit 8 which are adapted to select one gray shade voltage out of 128 gray shade voltage outputted from the gray shade voltage generating circuit 6 based on high order 7 bits of the digital image data transferred from the data latch circuit 3. Into the first gray shade voltage selecting circuit 7 is inputted a positive gray shade voltage and into the second gray shade selecting circuit 8 is inputted a negative gray shade voltage. Furthermore, the driving circuit is provided with a first output circuit 9 and a second output circuit 10 in which operational amplifiers are built in and an

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impedance of a signal outputted from the first gray shade voltage selecting circuit 8 is converted. Between the first gray shade voltage circuit 8 and the first output circuit 9/second output circuit 10 are analog switches 60, 61 used to select connections between them. The latch control signal STB and polarity signal POL are inputted into the first output circuit 9 and second output circuit 10 from the latch control circuit 5 and the least significant bit of the digital image data is inputted from the data latch circuit 3.

In the third full paragraph of page 21 (which bridges over to page 22), please delete that paragraph and replace it with the following:

According to the second embodiment, the driving circuit is provided additionally with an operational amplifier 21 connected to the positive polarity gray shade voltage selecting circuit 7 and an operational amplifier 22 connected to the negative polarity gray shade voltage selecting circuit 8. Moreover, to output terminals of the operational amplifiers 21 and 22 are connected output offset control circuits 23 and 24 through analog switches 60, 61. These output offset control circuits 23 and 24 have the same configurations as the output offset circuit 14 of the first embodiment. To these output offset control circuits 23 and 24 are connected output terminals to be connected to the display device such as TFT liquid crystal display panels or the like.

In the first full paragraph of page 22, please delete that paragraph and replace it with the following:

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According to the second embodiment, analog switches 60, 61 used to make a switching between the first gray shade voltage selecting circuit 7 and the second gray shade voltage selecting circuit 8 and between the output offset control circuit 23 and 24 have the same function as the resistor 12 mounted within the output circuit of the first embodiment, That is, gray shades are adjusted by using a voltage rise or drop generated by the analog switches 60, 61. Because of this, in the first embodiment, any component that can be a resistance component may be the resistor 12, however, in the second embodiment, unless the component is an analog switch, the liquid crystal display device is not driven in dot reverse.

In the last paragraph of page 23 (which bridges over to page 24), please delete that paragraph and replace it with the following:

Moreover, the driving circuit of this embodiment is provided with a first gray shade voltage selecting circuit 31 and a second gray shade voltage selecting circuit 32 adapted to select one gray shade voltage out of 128 gray shade voltages outputted from the gray shade voltage generating circuit 35 based on the digital image data transferred to the data latch circuit 36. The first gray shade voltage selecting circuit 32 are provided with transfer-gate type analog switches composed of p-channel transistors and n-channel transistors as illustrated in Figures 12. It also has a first output circuit 33 used to convert an impedance of a voltage outputted from the first gray shade selecting circuit 31 and a second output circuit 34 used to convert an impedance of a voltage outputted from the second gray shade selecting circuit 32. Configurations of the first output circuit 33 and the second output circuit 34 are the same as the output circuit in the first

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embodiment. However, to the LSB (Least Significant Bit) control circuit built in these circuits are inputted the least significant bit LSB of the digital image data and the latch signal STB only.

IN THE CLAIMS:

Please enter the following amended claims:

1. (Amended) A driving circuit of a display device for displaying a plurality of gray shades based on inputted digital image data comprising:

gray shade voltage generating means for generating a plurality of voltages;

gray shade voltage selecting means for selecting one voltage out of a plurality of voltages supplied from said gray shade voltage generating means based on high order bits composed of [one or two and more bits] at least one bit counted from the most significant bit of said digital image data and the number of bits of which is smaller than that of said digital image data, and for outputting said voltage;

an operational amplifier used to [convert an impedance of]amplify a voltage outputted from said gray shade voltage selecting means; and

voltage adjusting means for inducing a voltage rise or a voltage drop of a voltage outputted from said operational amplifier based on low order bits of said digital image data excluding said high order bits.

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